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APPLICANTS

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** CONTINUING DATA *****

This application is a DIV of 09/959,576 10/30/2001 ABN
 which is a 371 of PCT/JP99/02315 04/30/1999

YES LV

** FOREIGN APPLICATIONS *****

NONE LV

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 01/30/2004

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR COUNTRY JAPAN	SHEETS DRAWING 35	TOTAL CLAIMS 37	INDEPENDENT CLAIMS 6
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged	Examiner's Signature <i>[Signature]</i>	Initials LV		

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TITLE

Method of manufacturing a semiconductor integrated circuit device having a plurality of wiring layers and mask-pattern generation method

FILING FEE	FEES: Authority has been given in Paper	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of
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